CLAIMS

What is claimed is:

1. A smart card apparatus, comprising:

a processor;

a status register coupled to the processor to store status information indicative of a status associated with the processor; and

control logic coupled to the processor and to the status register to check the status information stored therein to determine the status of the processor, wherein if the control logic determines that the status information indicates a non-responsive state associated with the processor, the control logic can initiate a reset signal to the processor to remove the processor from the non-responsive state.

2. The apparatus of claim 1 wherein the non-responsive state comprises a mute mode.

3. The apparatus of claim 1 wherein the processor, status register, and control logic comprise part of a universal serial bus (USB)-compliant smart card.

4. The apparatus of claim 1, further comprising reset logic coupled between the control logic and the processor to provide the reset signal to the processor.

5. The apparatus of claim 4, further comprising:

a power on reset circuit, having an output terminal coupled to a first input terminal of the reset logic, to provide a first input signal to the reset logic to allow the reset logic to generate the reset signal in response thereto;

a second input terminal of the reset logic coupled to an output terminal of the control logic to receive a second input signal from the control logic;

a vendor specific request (VSR) block, having an output terminal coupled to a first input terminal of the control logic, to decode a received VSR and to provide a corresponding VSR signal to the control logic to allow the control logic to generate the second input signal in response thereto; and

a second input terminal of the control logic coupled to the status register to receive the status information stored therein, wherein the control logic can generate the second input signal to the reset logic if the status information is indicative of the non-responsive state.

6. The apparatus of claim 5 wherein the reset logic comprises an OR gate.

7. The apparatus of claim 1, further comprising:

a first line coupled between the processor and the status register to allow the processor to provide the status information to an element of the status register in a manner that the element is indicative of the non-responsive status;

a second line coupled between the control logic and the status register to allow the control logic to provide status information associated with the processor to the status register, after the processor has been removed from the non-responsive state; and

a third line coupled between the control logic and the status register to clear the element in the status register indicative of the non-responsive state.

8. The apparatus of claim 7 wherein the element of the status register comprises a bit that can be set.

9. A smart card system, comprising:

a means for storing processor status information;

a means for checking the stored processor status information to determine if a processor has entered a non-responsive mode; and

a means for automatically resetting the processor from the non-responsive mode, if the stored processor status information indicates that the processor has entered the non-responsive mode.

10. The system of claim 9, further comprising:

a means for providing external information to the processor and for receiving information from the processor;

a means for communicating between the means for providing external information and the processor;

a means for receiving the external information from the means for communicating; and

a means for routing and for buffering the received external information.

11. The system of claim 9, further comprising a means for updating the processor status information before the processor has entered the non-responsive mode and after the processor has been reset from the non-responsive mode.

12. The system of claim 9, further comprising either one or both:

a means for resetting the processor based on supplied power; and

a means for resetting the processor based on a request.

13. A method usable for a smart card, the method comprising:

storing status information associated with a state of a processor;

checking the stored status information to determine if the status information indicates that the processor has entered a non-responsive state; and

if the status information indicates that the processor has entered the non-responsive state, automatically resetting the processor to remove it from the non-responsive state.

14. The method of claim 13 wherein checking the stored status information to determine if the status information indicates that the processor has entered the non-responsive state comprises checking the stored status information to determine if the processor has entered a mute mode.

15. The method of claim 13 wherein storing status information associated with the state of a processor comprises setting a bit prior to the processor's entry into the non-responsive state.

16. The method of claim 13, further comprising:

updating the status information to indicate that the processor is reset from the non-responsive state; and

clearing any of the status information that is indicative of the non-responsive state.

17. The method of claim 13, further comprising at least one of the following:

resetting the processor in response to a first signal associated with power supplied to the processor; and

resetting the processor in response to a specific request received from a host device to reset the processor.

18. An article of manufacture, comprising:

a machine-readable medium having instructions stored thereon to:

store status information associated with a state of a processor;

check the stored status information to determine if the status information indicates that the processor has entered a non-responsive state; and

automatically reset the processor to remove it from the non-responsive state, if the status information indicates that the processor has entered the non-responsive state.

19. The article of manufacture of claim 18 wherein the machine-readable medium further includes instructions stored thereon to:

update the status information to indicate that the processor is reset from the non-responsive state; and

clear any of the status information that is indicative of the non-responsive state.

20. The article of manufacture of claim 18 wherein the machine-readable medium further includes instructions stored thereon to:

reset the processor in response to a first signal associated with power supplied to the processor; and

reset the processor in response to a specific request received from a host device to reset the processor.

21. The article of manufacture of claim 18 wherein the instructions to check the stored status information include instructions to regularly poll a data repository to obtain the status information.

22. The article of manufacture of claim 18 wherein the instructions to check the stored status information include instructions to review the status information after it has been updated in response to a change in status.

23. A smart card apparatus, comprising:

a processor; and

a device controller that can perform register-based and interrupt-based communication with the processor, the device controller including:

a status register coupled to the processor to store status information indicative of a status associated with the processor; and

control logic coupled to the processor and to the status register to check the status information stored therein to determine the status of the processor, wherein if the control logic determines that the status information indicates a non-responsive state associated with the processor, the control logic can initiate a reset signal to the processor to remove the processor from the non-responsive state.

24. The apparatus of claim 23 wherein the control logic can initiate the reset signal and a current configuration and state of the device controller is maintained.

25. The apparatus of claim 23 wherein the status register includes:

a first bit that can be set to indicate that the processor is to enter the non-responsive state and can be cleared if the processor has been removed from the non-responsive state; and

a second bit that can be used to track a history of non-responsive states of the processor.

26. The apparatus of claim 25, further comprising:

a first line coupled between the processor and the status register to allow the processor to set the first bit of the status register;

a second line coupled between the control logic and the status register to allow the control logic to set the second bit each time the processor is removed from non-responsive states; and

a third line coupled between the control logic and the status register to allow the control logic to clear the first bit after the processor has been removed from the non-responsive state.

27. The apparatus of claim 23 wherein the device controller comprises part of a USB-compliant smart card, and wherein the non-responsive state comprises a mute mode.